Amendments to the Claims:

This listing of claims replaces all prior versions and listings of claims in the application.

Listing of Claims:

1. (Original) An application specific integrated circuit (ASIC) comprising:

a standard cell, the standard cell including a plurality of logic functions;

at least one bus coupled to at least a portion of the logic functions;

a plurality of internal signals from the plurality of logic functions; and

a field programmable gate array (FPGA) function coupled to the at least one bus and the plurality of internal signals, the FPGA function including a debug client function that observes and manipulates the at least one bus and the plurality of internal signals.

2. (Original) The ASIC of claim 1 wherein the at least one bus comprises an internal bus.

3. (Previously Presented) The ASIC of claim 2 wherein the debug client function observes and manipulates at least one of the plurality of logic functions on the standard cell.

4. (Original) The ASIC of claim 1 wherein the debug client function is programmed by a server.

5. (Original) The ASIC of claim 1 wherein the debug client function further includes:

an external communicator logic function for receiving and transmitting information to a server;

selector logic coupled to the at least one bus and the plurality of internal signals, and

an interface logic coupled between the external communicator logic and the selector logic for providing communication therebetween.

6. (Currently Amended) The ASIC of claim 5 wherein the interface logic comprises:

a storage logic function for storing a state of at least one signal from the selector logic and providing the state to a server;

a comparator logic function coupled to the storage logic function for comparing the at least one signal ~~signals of interest~~ from the selector block function; and

an output logic function coupled to the comparator logic function for controlling the plurality of internal signals on the ASIC.

7. (Original) The ASIC of claim 4 wherein the server utilizes the debug client to debug hardware within at least one of the plurality of logic functions.

8. (Original) The ASIC of claim 4 wherein the server utilizes the debug client to debug software within at least one of the plurality of logic functions.

9. (Currently Amended) A debug client function within an application specific integrated circuit (ASIC), the debug client function being within a field programmable gate array (FPGA) function, the client debug function comprising:

an external communicator logic function for receiving and transmitting information concerning a plurality of internal signals of the ASIC to a server;

selector logic coupled to at least one bus of the ASIC and the plurality of internal signals,

and

an interface logic coupled between the external communicator logic and the selector logic for providing communication therebetween,

wherein the at least one bus comprises an internal bus, and the debug client function observes and manipulates at least one of the plurality of internal signals of the ASIC.

10-11. (Cancelled)

12. (Original) The ASIC of claim 9 wherein the debug client function is programmed by a server.

13. (Currently Amended) The ASIC of claim 9 wherein the interface logic comprises:

a storage logic function for storing a state of at least one signal from the selector logic and providing the state to a server;

a comparator logic function coupled to the storage logic function for comparing the at least one signal ~~signals of interest~~ from the selector block function; and

an output logic function coupled to the comparator logic function for controlling the plurality of internal signals on the ASIC.

14. (Original) The ASIC of claim 12 wherein the server utilizes the debug client to debug hardware within at least one of the plurality of logic functions.

15. (Original) The ASIC of claim 12 wherein the server utilizes the debug client to debug software within at least one of the plurality of logic functions.

16. (New) An application specific integrated circuit (ASIC) comprising:

a standard cell including a plurality of functional units, each functional unit having an internal signal;

a bus coupled to at least a portion of the plurality of functional units;

a field programmable gate array (FPGA) coupled to the bus and the plurality of functional units, the FPGA including a debug client operable to directly observe and manipulate the bus and the internal signal of each of the functional units,

wherein each internal signal being directly observed and manipulated is external to the FPGA.

17. (New) The ASIC of claim 16, wherein the bus comprises an internal bus, the internal bus being internal to the ASIC and not being exposed via an I/O pin.

18. (New) The ASIC of claim 16, wherein the debug client is further operable to debug software within one of the plurality of functional units.

19. (New) The ASIC of claim 16, wherein the debug client is programmed by a server.